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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/656,982	09/05/2003	Shashi B. Sakhuja	CAT-00001	9744

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EXAMINER	
ENGLUND, TERRY LEE	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 02/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/656,982	SAKHUJA ET AL.	
	Examiner	Art Unit	
	Terry L. Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) *31-34* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21 and 25-30* is/are rejected.

7)☒ Claim(s) *22-24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09052003 &.* 04082004
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Restriction

The response to the restriction requirement submitted on Nov 30, 2004 elected Group I, claims 1-30 drawn to circuitry that require at least two floating gate transistors. Therefore, claims 31-34 in Group II have been withdrawn from consideration.

Specification

The disclosure is objected to because of the following informalities: Page 15, line 2 of paragraph 0053 should have --120-- instead of "130" to correctly identify the programming transistor. Page 16, paragraph 0060 has "172" and "171" reversed on lines 4 and 5, respectively. Lines 6-7 of paragraph 0062 (on page 17) should be clarified with respect to what NOR gate 193 receives as inputs. For example, it does receive the output of inverter 191, which is control signal CTRL, but it also receives the output of NAND gate 192. As presently written, it appears 193 only receives the inverter's output and signal CTRL. Appropriate corrections are required.

Claim Objections

Claims 20-21 are objected to because of the following informalities: Since claim 20 cites "the programming control circuit " on lines 1-2, it is suggested --circuit-- be added after "control" on line 2 of claim 19 for consistent labeling. Claim 20, line 3 "a control" should be --the control-- since the gate was previously cited on line 5 of claim 19. Appropriate corrections are required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-21, and 25-30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. The use of "floating gate" coupled to the transistor's control gate is misleading. For example, it is not understood in claim 1 (lines 7-9) how a floating gate can be floating if it is connected to the transistor's control gate. Unless the gates are actually placed in a high impedance situation (e.g. disconnected from any source of potential), both gates will have the same potential that is applied to the control gate, and therefore the gates will not be floating (e.g. insulated from any voltage potential). Since claim 1 recites three floating gates, it is not clear in claim 7 which one is being referred to by "the floating gate" (see line 10). Using the applicant's own Fig. 1 as a reference, "the second transistor" 120 is not connected to an input terminal of comparator 180 as lines 5-7 of claim 5 recite. Was --the third transistor-- meant? Claims 10 (lines 1-12), 15 (lines 5-7), 25 (lines 10-12), and 27 (lines 5-6) have the same type of "floating gate" problem as previously described with respect to claim 1. For example, if both the floating and control gates are connected together, how can the floating gate be considered "floating"?

Claims 1-5, and 10-14 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: how the third transistor actually relates to the first and second transistor.

Claim 7 recites the limitation "the reference voltage circuit" in line 4 with insufficient antecedent basis for this limitation in the claim.

Dependent claims carry over any rejection(s) from any claim(s) upon which they depend.

Claim Rejections - 35 USC § 103

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

In so far as being understood, claims 1-2, 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pathak et al. (Pathak), in view of Madurawe et al. (Madurawe). Pathak shows a flash memory in Fig. 2 comprising main memory array 13 with at least first/second transistors each having their own respective floating gate and control gate; and third transistor 51 that essentially comprises a third floating gate 53 electrically connected to third control gate 57 via line 59. [Although the reference discloses "reference transistor 51 does not have a floating gate" (e.g. see column 8, lines 15-16), its floating gate/control gate configuration corresponds to the floating gate/control gate configuration of transistor 130 shown in the applicants' own Fig. 1.] However, the reference does not clearly show or disclose the first/second floating gates

electrically coupled to each other. Fig. 7 of Madurawe shows an example of a memory cell comprising two transistors 710/715, wherein their respective floating gates are electrically connected via 735. The shared floating gates provide various advantages as disclosed on column 18,lines 29-60 (e.g. minimizes sizes of the topography steps, wherein the lines and conductors across an array to not become too thin; optimizes programming; achieves longer device lifespan; improves data retention; and increases performance). Therefore, it would have been obvious to one of ordinary skill in the art to apply the teachings of Madurawe to the circuit and array of Pathak. For example, various transistors within array 13 of Pathak could be paired, such as first/second transistors C00/C01 could have their floating gates electrically connected together, rendering claim 1 obvious. [Note: Madurawe's transistors 710/715 share a common connection to their gates, corresponding to the shared control gates of Pathak's transistors C00/C01.] The shared floating gates will provide the advantages previously described with respect to the Madurawe reference above. Since Pathak's transistors 51, C00, and C01 are all NMOS type transistors, they can be considered matched. Also, Pathak discloses the reference cell matches the architecture of any memory cell on column 9, lines 12-15, with the exception of the floating gate/control gate connection. Therefore, claim 2 is rendered obvious. It would be obvious to one of ordinary skill in the art to form the second floating gate on an oxide layer, and use a thinned portion of the oxide layer as a programming window, rendering claim 4 obvious. A thinned oxide portion is a well known means for allowing the floating gate to be programmed. Deeming the ground connection as an input terminal, and sense amplifier 23 as a comparator (e.g. see column 6, lines 41-43), both the first/second transistors C00/C01 are effectively coupled between the input terminal and first input terminal 19 of the comparator, and third transistor 51 is

coupled between the input terminal and second input terminal 39 of the comparator, thus rendering claim 5 obvious. Interpreting the modified Pathak circuit in another manner, one of ordinary skill in the art would understand the first-third transistors of Pathak would be formed, wherein each has its own floating gate and control gate. Using the teaching of Madurawe with respect to the first/second transistors, they would have their floating gates electrically connected together. Since Pathak shows control gate 57 being effectively connected to floating gate 53 of third transistor 51, claim 10 is rendered obvious for similar reasons as previously described with respect to claim 1. Matched transistors 51 and C00 render claim 11 obvious for the same reasoning as previously applied to claim 2. Fabrication of a transistor using a thinned oxide layer and a floating gate is known to those of ordinary skill in the art. Therefore, the formation of the second floating gate on an oxide layer, with a thinned first portion (for programming purposes), is understood, rendering obvious claim 13. Also, due to their matched architecture, which will inherently include layered construction, it would be obvious to one of ordinary skill in the art to form the first-third floating gates during a first polysilicon process step, and the first-third control gates during a second polysilicon process step, and claim 14 is rendered obvious. [Note: Since the floating gate is an internal type layer, and a control gate is an external type layer, the internal layer would have to be formed prior to subsequent layers.]

Allowable Subject Matter

Claims 22-24 are allowed. There is no motivation to modify or combine any prior art reference to ensure the steps within the comparing method of independent claim 22 are met.

Claims 15, 25, and 27 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action. There is

presently no strong motivation to modify or combine any prior art reference(s) to ensure: 1) the first/second transistors are coupled between the input terminal and their respect inputs of the comparator, wherein the second transistor has both its control gate and floating gate electrically connected to the input terminal as recited within claim 15; 2) the reference voltage is supplied to the control gate and floating gate of the third transistor, as well as to the drains of the second and third transistors, as recited within claim 26; and 3) the intended relationships between the first/second transistors, with respect to the test voltage input terminal, as claim 27 apparently attempts to recite.

Claims 3, 6-9; 12, 16-21, 26, and 28-30 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims. There is presently no strong motivation to ensure: 1) the second transistor has a gate area substantially larger than its channel area as recited within claim 3; 2) the third control gate is connected to the input terminal as recited within claim 6 (upon which claims 7-9 depend); and 3) the second floating gate is larger than the first floating gate as recited within claim 12. Claims 16-21 carry over the rejection of their independent claim 15; claim 26 carries over the rejection from independent claim 25; and claims 28-30 carry over at least the rejections from independent claim 27.

Prior Art

The other prior art references cite don the accompanying PTO-892 are deemed relevant to at least sections of the claimed invention. Nazarian shows and discloses examples of two transistors sharing a common connection with respect to their floating gates. For example, see Figs. 11 and 12. Okamoto et al. shows a comparator coupled to two transistors in Fig 3, wherein

each transistor has its own floating gate, and the other end of each transistor is coupled to common input voltage VDD. However, neither of these references show/disclose the first-third (or first/second) transistor combinations, or method steps, that the claims either recite, or is understood as attempting to recite (e.g. using the applicants' own figures as a reference).

The prior art references cited on the IDS forms submitted Sep 5, 2003 and Apr 8, 2004 were reviewed and considered. None of these references clearly show or disclose the recited transistor combinations, and/or method steps, either.

Any inquiry concerning this communication, or previous communications, from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (571) 272-1740.

The new central official fax number is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLE

Terry L. Englund
31 January 2005

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